IN THE CLAIMS

1-8. (Cancelled)

9. (Currently Amended) A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag address storage locations; and

a system memory coupled to the memory controller, the system memory including at least two memory modules, each memory module including

at least one bank of memory devices, and

a memory module buffer having a data cache coupled to an eviction buffer, both coupled to the bank of memory devices, the memory module buffer including a command deserializer and decoder unit to control the data cache and the eviction buffer according to ~~controlled by~~ a plurality of commands delivered by the memory controller, the commands sequentially delivered over a plurality of transfer periods of a memory access transaction, the plurality of commands including an activate command and a writeback command, the memory controller to issue a write transaction, the command deserializer and decoder unit to store ~~writing~~ a current line of data ~~to~~ within the data cache~~,~~ until the memory controller signals an eviction, the command deserializer and decoder unit to ~~further~~ instruct the data cache to evict the current cache ~~a previous~~ line of data from the data cache into the eviction buffer.

10. (Cancelled)

11. (Currently Amended) The system of claim 9, the memory controller to deliver ~~a~~ the writeback command to the command deserializer and decoder unit ~~data cache~~, the ~~writeback~~ command deserializer and decoder unit to cause the ~~previous~~ current cache line of data to be written out of the eviction buffer to the bank of memory devices, the memory controller to issue the activate command if a row for the current cache line is not open.

12. (Currently Amended) The system of claim 11, the writeback command including way information and bank address information delivered during a last transfer period of the plurality of transfer periods.

13-15. (Cancelled)

16. (Currently Amended) A memory controller, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache and an eviction buffer located on a memory module buffer of at least one memory module of a system memory by delivering a plurality of commands over a plurality of command and address lines, the commands sequentially delivered over a plurality of transfer periods of a memory access transaction, the plurality of commands including an activate command and a writeback command, the command sequencer and serializer to deliver a writeback command to the eviction buffer associated with the memory module, the writeback command to cause a previous line of data evicted from the data cache and stored in the eviction buffer, to be written out to a memory device of the memory module.

17. (Currently Amended) The memory controller of claim 16, wherein the memory controller to issue an eviction signal to the data cache to evict the previous line of data from the data cache into the eviction buffer, the memory controller to issue the activate command if a row for the current cache line is not open.

18. (Currently Amended) The memory controller of claim 16, wherein the memory controller issues the writeback command to cause the previous line of data to be written out of the eviction buffer to the memory device once the memory device is idle, the memory controller to issue the activate command if a row for the current cache line is not open.

19. (Previously Presented) The memory controller of claim 16, wherein the command sequencer and serializer unit to cause a current line of data to be written from the

command sequencer and serializer unit to the data cache, the command sequencer and serializer unit to cause the previous line of data to be evicted out of the data cache to the eviction buffer located on the memory module.

20. (Currently Amended) A memory module, comprising:

at least one bank of memory devices; and

a memory module buffer having a data cache coupled to an eviction buffer, both coupled to the bank of memory devices, the memory module buffer including a command deserializer and decoder unit to control the data cache and the eviction buffer according to ~~controlled by~~ a plurality of commands delivered by a memory controller over a memory bus, the commands sequentially delivered over a plurality of transfer periods of a memory access transaction, the plurality of commands including an activate command and a writeback command,

the command deserializer and decoder unit ~~the memory module~~ to receive a writeback command, the command deserializer and decoder unit ~~writeback command~~ to cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the bank of memory devices.

21. (Currently Amended) The memory module of claim 20, wherein the data cache to evict the previous line of data from the data cache into the eviction buffer according to an eviction signal received from the memory controller, the memory controller to issue the activate command if a row for the current cache line is not open.

22. (Currently Amended) The memory module of claim 20, wherein the writeback command including way information and bank address information delivered during a last transfer period of the plurality of transfer periods.

23. (Currently Amended) A system memory comprising:

at least two memory modules, each memory module including:

at least one bank of memory devices, and

a memory module buffer, having a data cache coupled to an eviction buffer, both coupled to the bank of memory devices, the memory module buffer including a command

deserializer and decoder unit to control the data cache and the eviction buffer according to a plurality of commands delivered by a memory controller, the commands sequentially delivered over a plurality of transfer periods of a memory access transaction, the plurality of commands including an activate command and a writeback command, the eviction buffer to store one or more lines of data evicted from the data cache.

24. (Currently Amended) The system memory of claim 23, wherein the command deserializer and decoder unit ~~a memory module~~ to receive a writeback command issued by the memory controller, the ~~writeback command~~ command deserializer and decoder unit to cause a previous line of data, evicted from the data cache, to be written out of the eviction buffer to the bank of memory devices of the memory module, the memory controller to issue the activate command if a row for the previous line of data is not open.

25. (Currently Amended) The system memory of claim 23, wherein the~~a memory module~~ command deserializer and decoder unit to store a current line of data within ~~a~~ the data cache of the memory module, the ~~memory module~~ command deserializer and decoder unit to evict the previous line of data from the data cache to the eviction buffer located on the memory module buffer in response to a received eviction signal.